CC120/1/2

BOARD USER MANUAL

ALS 50267 c-en

FOREWORD

This document is part of the ALSTOM technical documentation. It is regularly updated, in particular for all sub-assemblies containing micro-programmed software.
The user of this document should take care to check that it corresponds to the hardware and software versions of the product on which he or she is working.

This manual will best be used concurrently with the other documents supplied on delivery.

REVISION TABLE

Index letter	Date	Nature of revision
b	12-1994	Integration of 2.5 Mbs version.
c	02-2000	ALSTOMISATION

A "remarks" form is included at the end of this manual. Please return this form promptly as indicated if you have any suggestions for improvements or other comments.

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YOUR COMMENTS ON THIS DOCUMENT

TITLE

CC120/1/2
BOARD USER MANUAL

REFERENCE No.

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SUGGESTED IMPROVEMENTS

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1 - GENERAL PRESENTATION

1.1 - INTRODUCTION

The CC120/1/2 boards family permits to realize the connection between any IBM compatible personal computer with ISA 8 bis short format extension slot, and the serial FIP/WORLDFIP bus. The board must be plugged into one of the PC I/O (input/output) bus connectors.

1.2 - BOARD FEATURES

1.2.1 - CC120

• Physical layer conformant to the WORLDFIP physical layer standard : IEC 1158-2, 31.25 Kbs voltage mode with isolating transformer coupling.

• FULLFIP2 communication coprocessor running at 40 MHz.

• FULLFIP2 private memory : static RAM of 128K x 16 bits.

• Medium Attachment Unit (MAU) solution based on FIELDRIVE + FIELDTR31.25 components.

• Bimedium option (CC120). The bimedium option is based on the ZN130 software item associated to a standard INTEL-NPL910 programmable device.

• 2 interrupt lines :
  • IRQFIP   (interruption generated by the IRQN and EOC interrupt signals from FULLFIP2),
  • WDG   (' watchdog' generated by the FIELDRIVE circuits).

1.2.2 - CC120-1

• Momedium board derivated from the CC120 board. One single MAU solution with FIELDRIVE + FIELDTR31.25 is directly interfaced with FULLFIP2 coprocessor.

• Other features are fully identical with those of the CC120 board.

1.2.3 - CC121

• Physical layer is conformant to the WORLDFIP physical layer standard : IEC 1158-2, 1Mbs voltage mode with isolating transformer coupling; and also conformant to the FIP physical layer standard : UTE C46-604, 1Mbs.

• FULLFIP2 communication coprocessor running at 64 MHz.

• Other features are fully equivalent with those of the CC120 board.

1.2.4 - CC121-1

• Momedium board derivated from the CC121 board. One single MAU solution with FIELDRIVE + FIELDTR31.25 is directly interfaced with FULLFIP2 coprocessor.

• Other features are fully identical with those of the CC121 board.

1.2.5 - CC122

• Physical layer is conformant to the WORLDFIP physical layer standard : IEC 1158-2, 2.5Mbs voltage mode with isolating transformer coupling; and also conformant to the FIP physical layer standard : UTE C46-604, 2.5Mbs.

• FULLFIP2 communication coprocessor running at 80 MHz.

• Other features are fully equivalent with those of the CC120 board.

1.2.6 - CC122-1

• Momedium board derivated from the CC121 board. One single MAU solution with FIELDRIVE + FIELDTR2.5 is directly interfaced with FULLFIP2 coprocessor.

• Other features are fully identical with those of the CC121 board.

1.3 - DIAGRAM: BIMEDIUM SOLUTIONS CC120, CC121 AND CC122

ISA bus 8 bits

Interface

FULLFIP2

Private
RAM

ZN130 + NPLD910
Medium
Redundancy

FIELDRIVE

FIELDRIVE

FIELDTRx

FIELDTRx

Note : x = 31.25 or 1 or 2.5

Note : x = 31.25 or 1 or 2.5

FIP cable channel 1

FIP cable channel 2
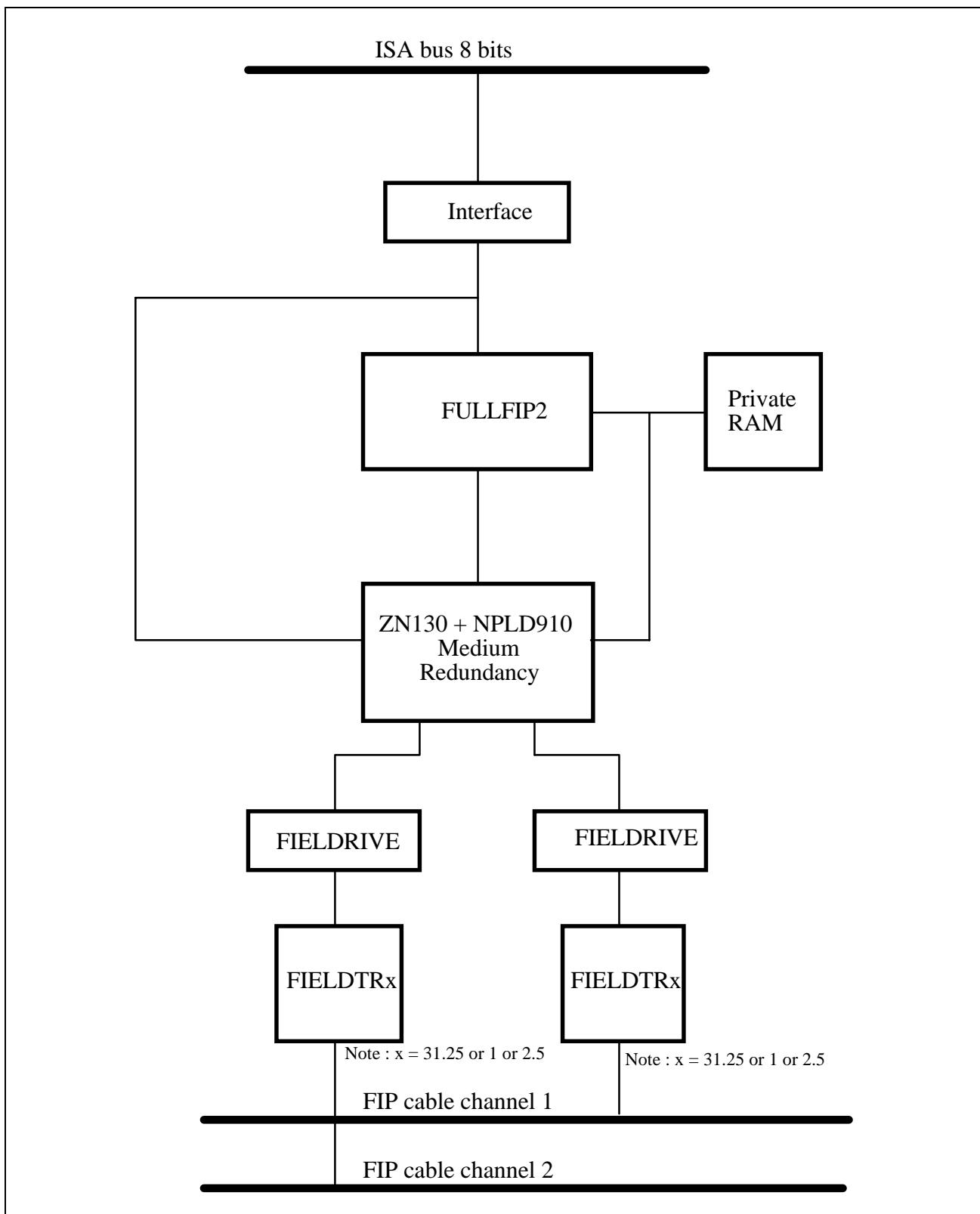
1.4 - DIAGRAM: MONOMEDIUM SOLUTIONS CC120-1, CC121-1 AND CC122-1

ISA bus 8 bits

Interface

FULLFIP2 ——— Private RAM

FIELDRIVE

FIELDTRx

x = 31.25 or 1 or 2.5

FIP cable
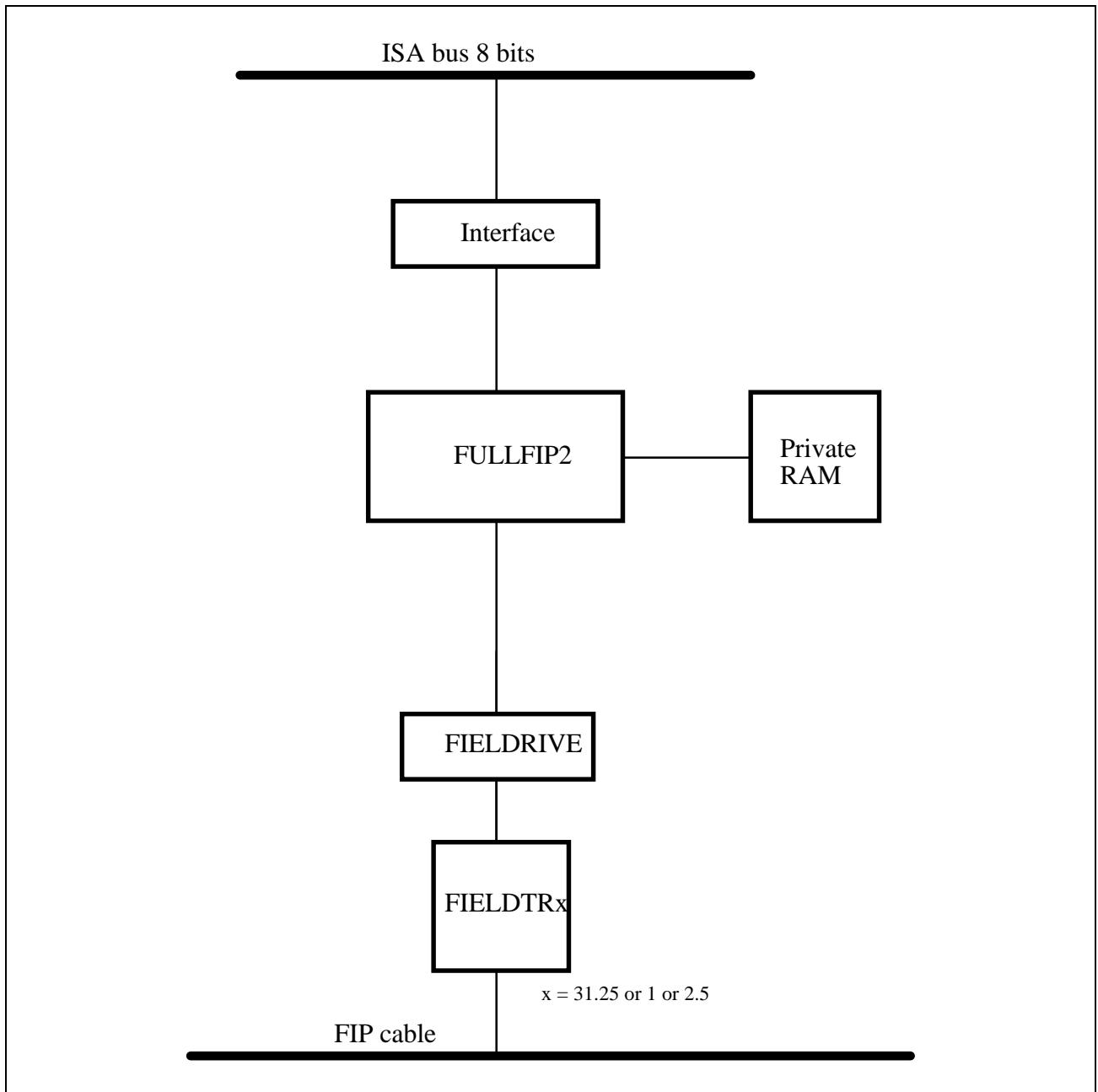
2 - BOARDS FUNCTIONALITIES

2.1 - IBM PC BUS SIGNALS

(Only signals which are used by the CC120/1/2 boards are mentionned below.)

- CLK (clock) :
  clock synchronized with the bus control signals,

- RESET DRV (reset driver) :
  signal of reset of the input/output bus (active when '1') ,

- Aø à A19 :
  address lines,

- Dø à D7 :
  data lines,

- ALE (address latch enable) :
  signal indicating the validity of the address present on the input/output bus (active when '1'),

- I/OCHCK (I/O channel check) :
  signal indicating an error on an input/output board and involving a non masquable interruption of the PC processor (active when 'Ø'),

- I/OCHRDY (I/O channel ready) :
  signal permitting to insert wait states (Tw) within a bus cycle when the addressed peripheral is not fast enough (active when 'Ø'),

- IRQ3 to IRQ7 and IRQ9 (interrupt requests) :
  these 6 signals permit to send interruptions to the PC processor (active when '1'),

- IOR (I/O read) :
  signal indicating to the input/output peripherals that the PC processor is performing a read cycle (active when 'Ø'),

- IOW (I/O write) :
  signal indicating to the input/output peripherals that the PC processor is performing a write cycle (active when 'Ø'),

2.2 - **FULLFIP2 COPROCESSOR**

The FULLFIP2 communication coprocessor is managed by the PC by mean of its write and read registers. On CC120 boards, FULLFIP2 is driven by a 40 MHz oscillator and is configured for network operations at 31.25 KBit/s. On CC121 boards, FULLFIP2 is driven by a 64 MHz oscillator and is configured for network operations at 1 MBit/s. On CC122 boards, FULLFIP2 is driven by a 80 MHz oscillator and is configured for network operations at 2.5 MBit/s.

Every access to the FULLFIP2 registers is performed in an asynchronous mode, and the end of each access to the FULLFIP2 registers are qualified by the CC120/1/2 boards which manage the I/OCHRDY acknowledge signal on the ISA bus.

FULLFIP2 is equiped with a private memory of 128K x 16 bits, that contains the microcode to be exercised, which is loaded by the PC during the system initialisation phase, and also contains the network data base contents.

2.3 - **MEDIUM ATTACHMENT UNIT SOLUTION**

The Medium Attachment Unit function (MAU) is realised by using the FIELDRIVE circuit (line driver) and the FIELDTR31.25 or FIELDTR1 or FIELDDTR2.5 transformers, respectively for the CC120, CC121 and CC122 boards.

FIELDRIVE diagnosis features such as Manchester symbol checking, overload and underload detections, and lastly jabbering detection are performed on the CC120/1/2 boards. The last condition causes WDG error condition when it is encountered.

The CC120/1/2 boards can be operated correctly on well adapted networks only. Adaptation circuits will be selected as conformant with the corresponding normalisation requirements, that must be considered as specific for each network bit rate.

External passive elements associated to FIELDRIVE, as well as protection elements are specifically targetted for each network bit rate.

2.4 - MEDIUM REDUNDANCY MANAGEMENT (BIMEDIUM BOARDS)

The ZN130 medium redundancy agent manages the transmission and the reception enabling on the two redundant medium. It works under the control of the host processor.

In normal conditions, transmission is performed simultaneously on both mediums, and reception is selected from the first medium that provides the carrier detection information.

The agent collects errors from MAU circuitry, that are the jabbering detection and the transmit error detection.

The error handling principle consists in disabling the channel giving the error indication, and providing the information to the user microprocessor that will control the channel enabling phase.

Features are integrated that prevent from full stopping on both channels when transmission errors are monitored on both channels and when jabbering conditions are none.

When handling reception operation, the agent doesn't perform any check on the received signal. This work is performed by the FULLFIP2 coprocessor.

Lastly, the aent integrates loopback modes that can be used to send back to FULLFIP2 each frame that was produced.

2.5 - INTERRUPTIONS

The CC120/1 boards can generate two interruptions :
• IRQFIP (interruption generated by the FULLFIP2 circuit lines EOC and IRQN).
• WDG ('watch-dog' generated by the MAU circuitry).

The logical 'or' of these two interruptions is connected to one of the 6 interrupt lines available on the PC I/O bus (IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, IRQ9) by using a jumper.

The initiator of the interruption (FULLFIP2 interruption or watchdog interruption) can be known by reading the status register.

2.6 - SUBSCRIBER NUMBER

The network subscriber number can be encoded on 8 bits by using the S5.1 to S5.8 switches. This information is provided to the PC as a readable register.

2.7 - HARDWARE VERSION

The hardware version number is encoded on 8 bits by the board cabling ; it can be read by the PC by selecting the corresponding register.

2.8 - FIELDRIVE MODES SELECTION

TS0 and TS1 control pins of each FIELDRIVE component can be programmed when accessing a specific register of the CC120/1/2 boards, then allowing to exercise each FIELDRIVE in one of its four available operating modes :
• normal mode,
• loopback mode,
• loopback mode with receive activity indication delayed,
• loopback mode with WDG watchdog error and TXER transmitter error activated.

2.9 - **BOARD STATUS INFORMATION**

The board status information is used to check:

• weither the board is under RESET or not,

• the status of each interrupt line: IRQN or EOC from FULLFIP2, WDG watchdog interruption from the MAUs circuitry,

• weither the board is monomedium or bimedium. (difference between CC120/1/2 boards and CC12/1/2-1 boards).

2.10 - **BOARD IDENTIFICATION**

Each board is associated to a specific identication number, that codes in hexadecimal the number of its name (ie. CC120 identification = 78 hex.).

Then the user has a full knowledge of the board caracteristics reading both the board status information and the board identification registers.

3 - **PROGRAMMING MODEL**

3.1 - **BOARD SELECTION**

The selection of the CC120/1/2 board is made by using six switches (S1.1 to S1.6) which are compared to the PC bus A6 to A11 addresses.

The A9 address bit must be set to '1' (the addresses from **0000**H to **01FF**H being reserved for the PC system).

The A1Ø and A11 address bits can be used when the CC120/1/2 board has to be plugged into an extension of the PC input/output bus.

Anyway most applications will be satisfied by placing respectively A9, A10, and A11 at values 1, 0, and 0.

6	5	4	3	2	1	S1 switches
A11	A10	A9	A8	A7	A6	Adress bits
0	0	1	X	X	X	Selection

3.2 - GLOBAL FUNCTIONS DECODING

The A3 and A4 address decoding validated by the board select signal and the ALE signal (valid addresses) provides the select signals of the different board functions.

• FULLFIP2 selection in registers access mode.

• Software initialisation management, access to subscriber number and hardware identification information.

• FIELDRIVE modes selection, access to board status information.

• Medium redundancy management (CC120/1/2 bimedium options only).

A5	A4	A3	Access selected
0	0	0	FULLFIP2 registers
0	0	1	Software initialisation, Subscriber number, & Hardware identifica-tion.
0	1	0	FIELDRIVE modes selection, board status informa-tion, board identification.
0	1	1	Reserved.
1	0	0	Medium redundancy management (bime-dium boards only).

3.3 - DETAILED FUNCTIONS DECODING

3.3.1 - FULLFIP2 registers

Selection with (A5 = A4 = A3 = 0).

ADRESSING:

A5	A4	A3	A2	A1	A0	READ registers	WRITE registers
0	0	0	0	0	0	U_STATE	U_COM
0	0	0	0	0	1	U_FLAGS	U_SWITCH
0	0	0	0	1	0	VAR_STATE	KEY_H (pF)
0	0	0	0	1	1	VAR_SIZE_L	KEY_L (pf)
0	0	0	1	0	0	VAR_SIZE_H	TIME_H (pF)
0	0	0	1	0	1	Reserved.	TIME_L (pf)
0	0	0	1	1	0	Reserved.	Reserved.
0	0	0	1	1	1	FILE	FILE

3.3.2 - **Software initialisation, Subscriber number, & Hardware identification**

Selection with (A5 = A4 = 0, A3 = 1).

ADRESSING:

A5	A4	A3	A2	A1	A0	READ registers	WRITE registers
0	0	1	0	0	0	Subscriber number	RESET desactivation.
0	0	1	0	0	1	Hardware identification	RESET activation.

3.3.3 - **FIELDRIVE modes selection, board status information, board identification**

Selection with (A5 = 0, A4 = 1, A3 = 0).

ADRESSING:

A5	A4	A3	A2	A1	A0	READ register	WRITE register
0	1	0	0	0	0	Board status information	FIELDRIVE mode selection
0	1	0	0	0	1	Board identification	

BOARD STATUS INFORMATION REGISTER FORMAT :

D7	D6	D5	D4	D3	D2	D1	D0
0	BIMEDIUM	EOC	0	RESET	0	WDG	IRQFIP

(Each bit placed at high level coreesponds to a signal active condition).

BOARD IDENTIFICATION REGISTER FORMAT:

D7	D6	D5	D4	D3	D2	D1	D0	Board identification
0	1	1	1	1	0	0	0	CC120
0	1	1	1	1	0	0	1	CC121
0	1	1	1	1	0	1	0	CC122
0	1	1	1	1	0	1	1	reserved

FIELDRIVE MODES SELECTION REGISTER FORMAT:

D5	D4	D1	D0
TS1	TS0	TS1	TS0
voie 2	voie2	voie1	voie1

(D5 and D4 not significant for monomedium boards, other bits reserved.)

TS1 TS0	FIELDRIVE mode description
0 0	normal mode
0 1	loopback mode
1 0	loopback mode with receiver activity delayed
1 1	loopack mode with WDGN and TXER errors activated.

3.3.4 - **Medium redundancy management (bimedium boards only)**

Selection with (A5 = 1, A4 = 0, A3 = 0).

ADRESSING:

| A5	A4	A3	A2	A1	A0	READ registers	WRITE registers
1	0	0	0	0	0	Channels 1 & 2 status register	loopback selection (Channels 1 & 2 disable)
1	0	0	0	0	1	Clear error command	Channel 1 enable Channel 2 disable
1	0	0	0	1	0	Reset channel 1 activation	Channel 1 disable Channel 2 enable
1	0	0	0	1	1	Reset channel 2 activation	Channels 1 & 2 enable

CHANNELS 1 & 2 ZN130 STATUS REGISTER FORMAT:

D7 & D6	D5	D4	D3	D2	D1	D0
reserved	EWD2	EWD1	ET2	ET1	VAL2	VAL1

4 - **NETWORK CONNECTION**

The CC120/1/2 bimedium boards are equipped with two isolated 9-point male SUBD connectors for connection with the FIP bus cable.

The monomedium boards CC120/1/2-1 are only equipped with one connector.

IBM PC bracket

P2 (male) 9-point
SUBD connector

D- (pin 7)
D+ (pin 6)
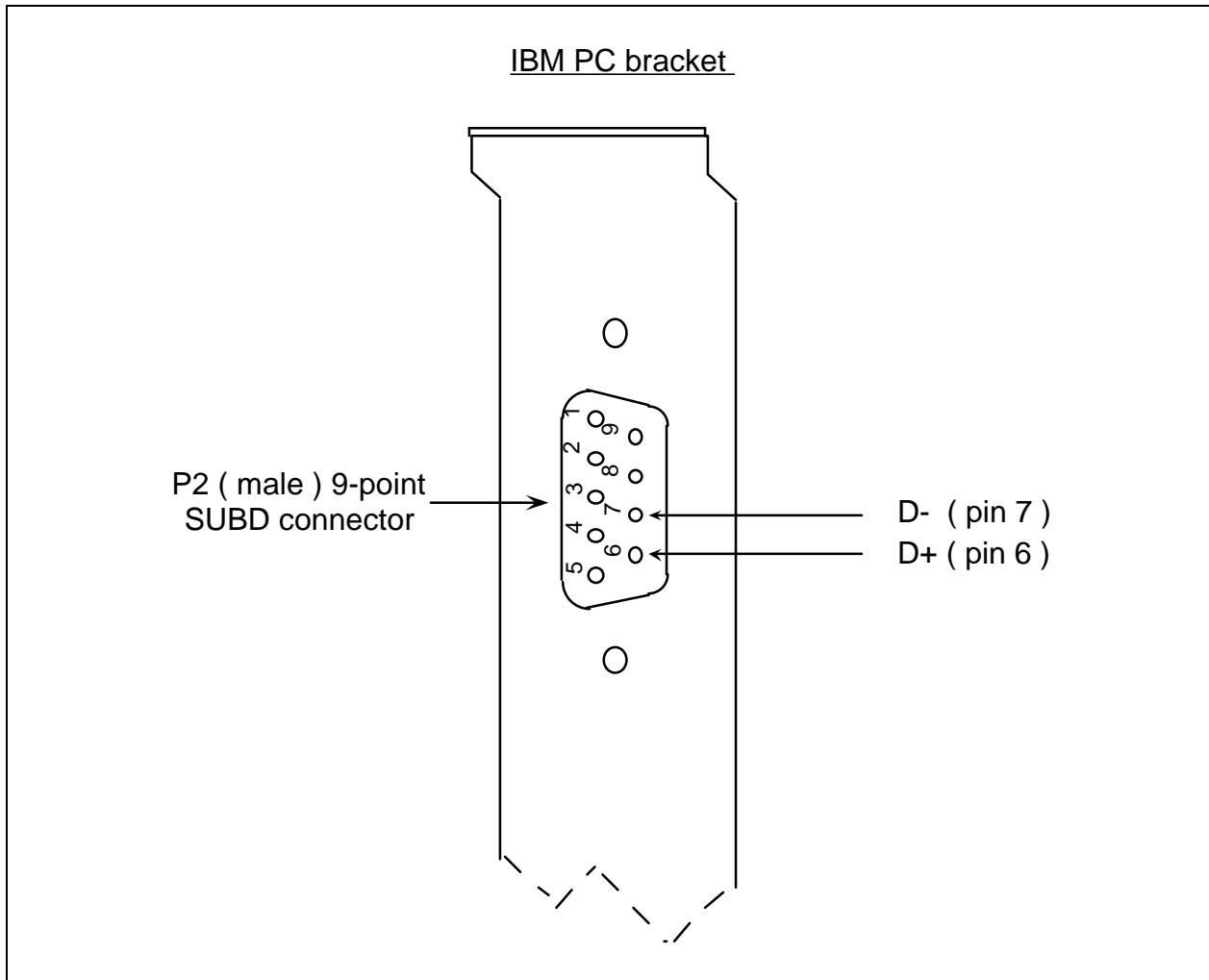
The CC120/1/2 boards are equipped with a bracket for IBM PC.

5 - HARDWARE CONFIGURATION

5.1 - BOARD LAYOUT

5.1.1 - CC120/1/2 Boards (bimedium)
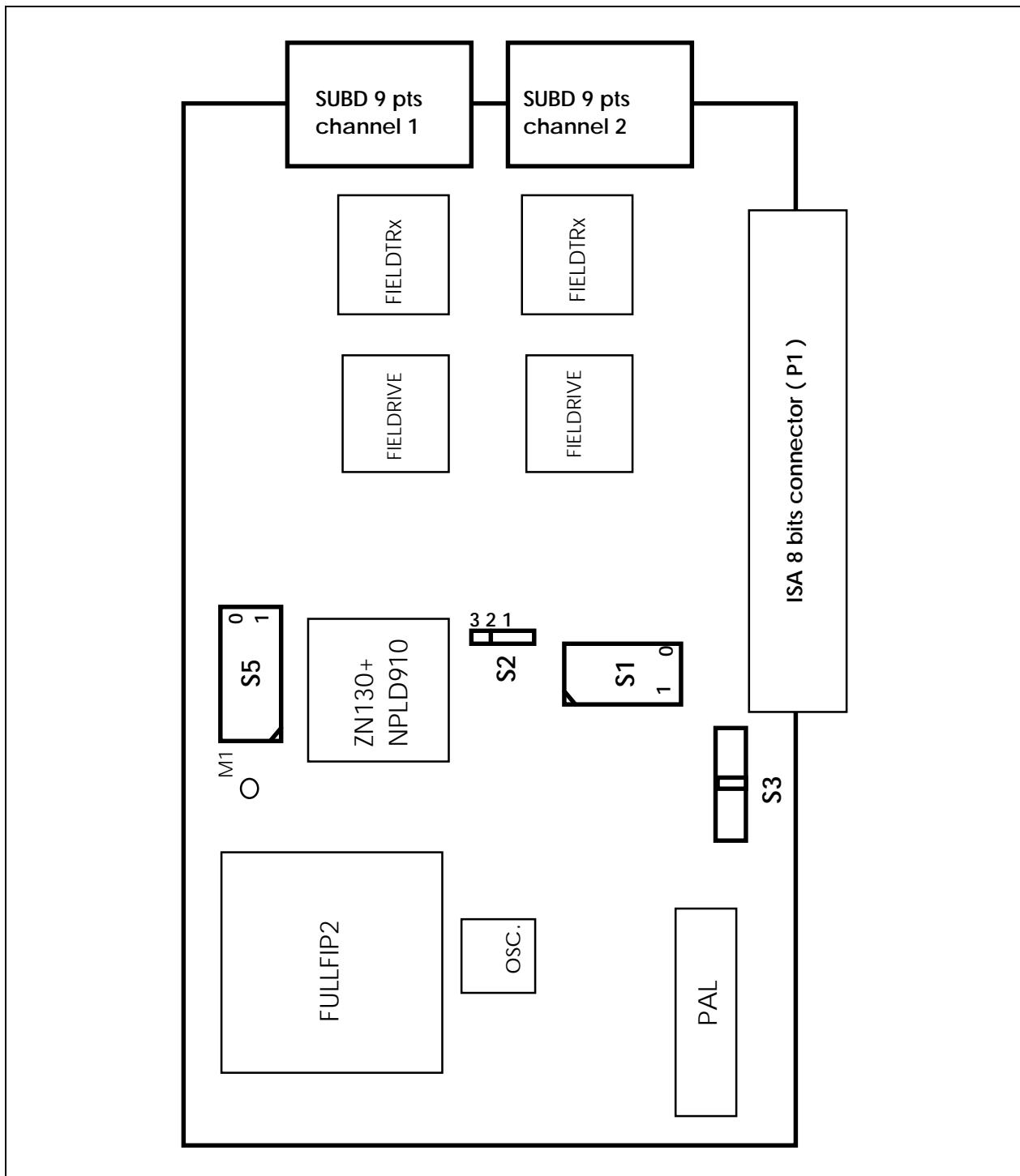
5.1.2 - CC120/1/2-1 Boards (monomedium)
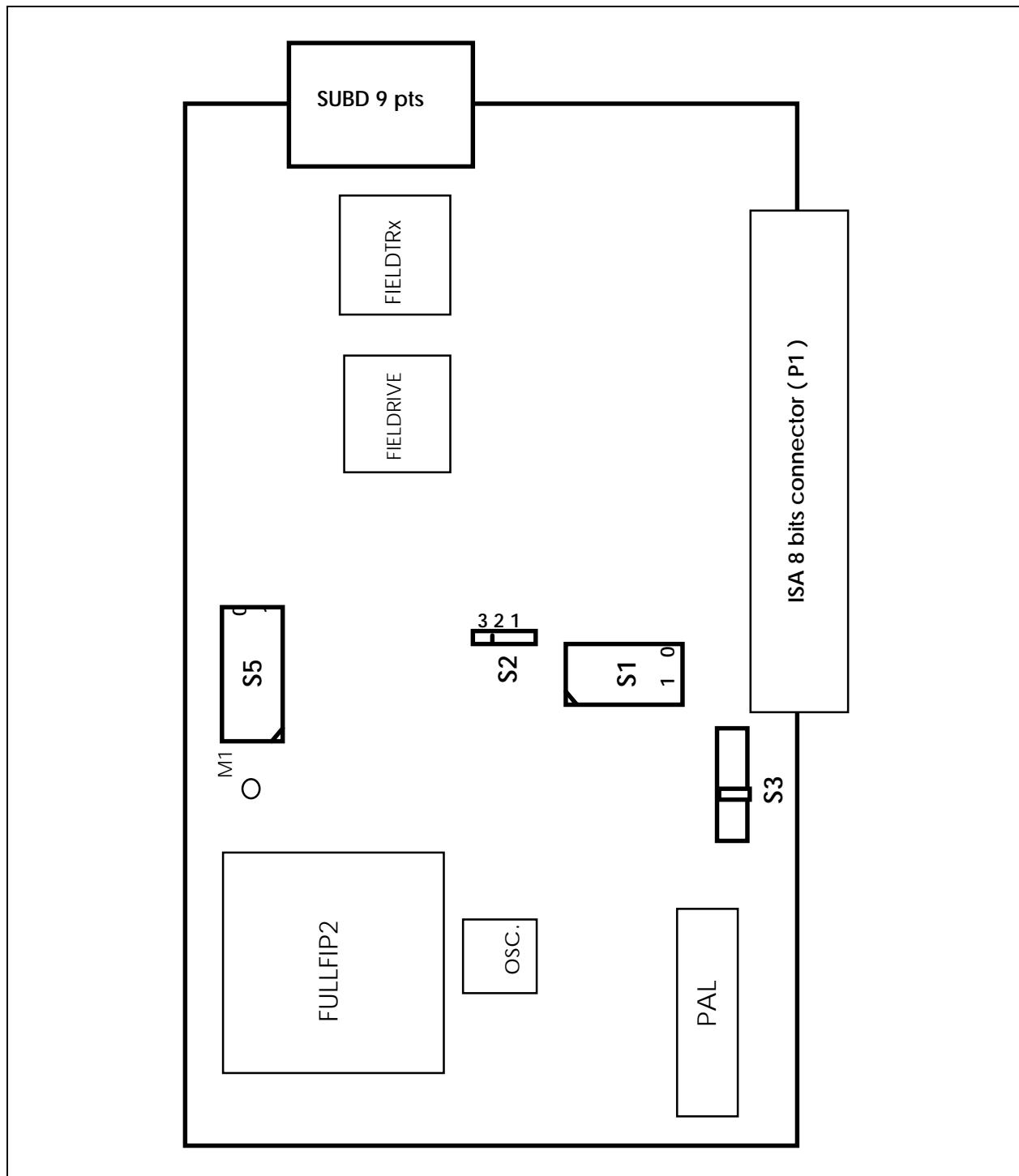
5.2 - JUMPERS CONFIGURATION

• **S2** : **WATCHDOG**

In 1-2 position this jumper directs the WDG signal towards an interrupt line of the PC bus,

In 2-3 position this jumper directs the WDG signal towards the I/OCHCK line of the PC bus,

• **S3** : **INTERRUPT LINE SELECTION**

This jumper permits to direct the interrupt signal of the CC120/1/2 board towards one of the 6 interrupt lines of the PC bus.
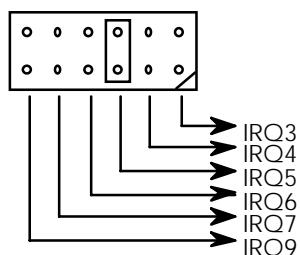
5.3 - **DIP SWITCH CONFIGURATION**

• **S1.1 à S1.6 :** **BOARD ADRESS.**

These seven DIP switches permit to encode the CC120/1/2 board address on the PC input/output bus.

S1

1	A6
2	A7
3	A8
4	A9
5	A10
6	A11
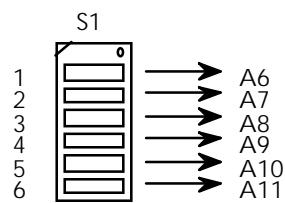
• **S5.1 à S5.8 :** **SUBSRIBER NUMBER ENCODING.**

These eight DIP switches permit to encode a user 8-bit value.

S5

1	DB7
2	DB6
3	DB5
4	DB4
5	DB3
6	DB2
7	DB1
8	DB0
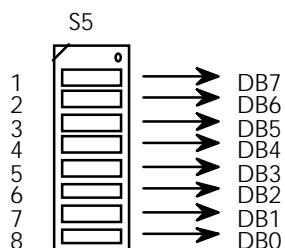
6 - PHYSICAL CHARACTERISTICS

6.1 - DIMENSIONS

The CC120/1/2 boards have the IBM PC plug-in board format with L = 171.5 mm.

6.2 - ENVIRONMENTAL CONDITIONS

The reference used will be the normalisation document NF C46-637 that specifies environmental requirements and test rules for the FIP network components.

- Operating temperature :   0 - 55°C.
- Relative humidity :   0 - 80 %.

6.3 - DYNAMIC CHARACTERISTICS

- Oscillator :   ± 50 ppm.

6.4 - ELECTRICAL CHARACTERISTICS

- Supply voltage   5V +/- 5% .
- Consumption   600 mA (typ.).